#11 Amdt Board 6/10/03 ars

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **OZAWA, Hiroyuki et al.**

Group Art Unit: **2815**

Serial No.: **09/994,753**

Examiner: **CLARK, SHEILA V.**

Filed: **November 28, 2001**

P.T.O. Confirmation No.: 8648

For: **SEMICONDUCTOR INTEGRATED CIRCUIT WITH DUMMY PATTERNS**

Dunker 8/5/3

RESPONSE UNDER 37 CFR §1.116
- EXPEDITED RESPONSE -
GROUP ART UNIT 2815

MAILSTOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

May 28, 2003

Sir:

In response to the Office Action dated **January 28, 2003**, extended to **May 28, 2003** by a one-month Petition for Extension of Time please amend the above-identified application as follows:

IN THE CLAIMS:

AMEND claims 1, 6 and 8 to read as follows:

B1

1. (AMENDED) A semiconductor integrated circuit, comprising:

a plurality of layers provided on a semiconductor substrate;

wires provided in a first layer that is one of said plurality of layers; and

wire dummies provided in a second layer different from the first layer by avoiding areas that are directly above or below positions of said wires provided in said first layer.